

General Description

PVG001 employs a pile of photovoltaic cells and control logic to generate proper voltage between G and GND, controlled by the input IR light; It can drive external power MOS transistors to implement solid state relay applications(SSR).

Chip Dimension

- Die size (Maximum): 1.42mm × 1.44mm (14 photovoltaic Cells, include scribe line)
- Die thickness: 300um
- Scribe line width: 70um
- Metallization:
 TOP: ALSI
 Back side: isolated(die attach using conductive epoxy)
- Passivation : $\text{SiO}_2 + \text{Si}_3\text{N}_4$
- Wire bonding: Au thermo sonic ball bonding
- Bond pad size(Minimum): 90 × 90um

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	-55 ~ 125	°C
Operating Temperature	T_{opr}	-55 ~ 105	°C

Electrical Characteristics

Parameter	Symbol	Unit	Criterion			Test Conditions	Measure Circuit
			Min	Typ	Max		
Open circuit Voltage	V_{oc}	V	6	7.5		(1)	Fig.1
Short Circuit Current	I_{sc}	μA	10	15		(1)	Fig.2
Turn-on Time	T_{on}	ms		0.5		(2)	Fig.3
Turn-off Time	T_{off}	ms		0.5	1		

Note:

- 1、 Use light Source with $\lambda=850\text{nm}$ $I_F=10\text{mA}$
- 2、 Use light Source pulse signal with $\lambda=850\text{nm}$ $I_F=5\text{mA}$, $f=2\text{KHz}$, 50% duty cycle, Measure T of V with $C_L=300\text{PF}$

Test Circuit

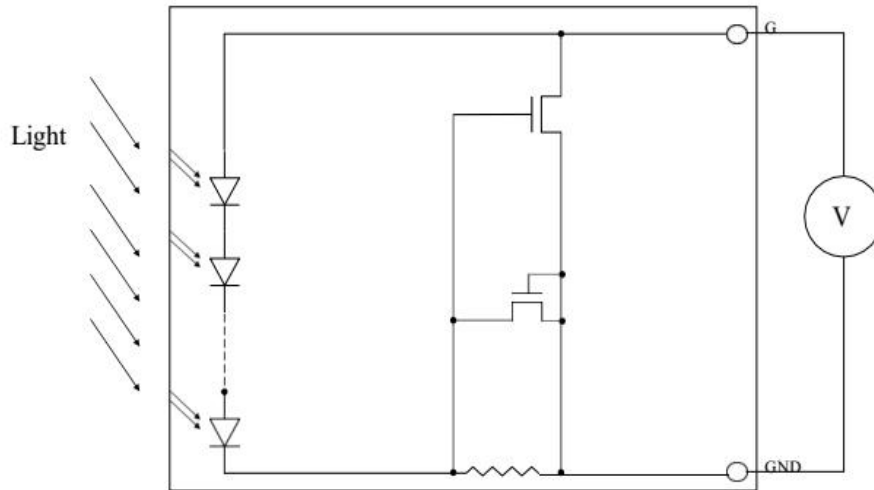


Fig1: Open Circuit Voltage Test Circuit

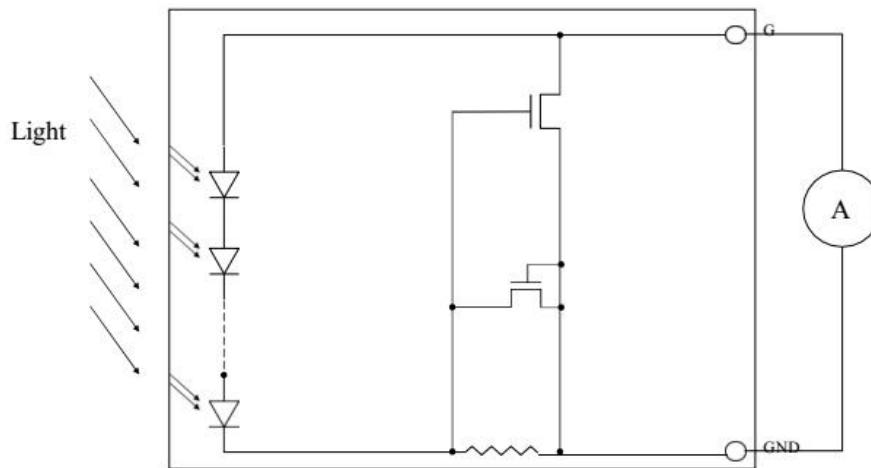


Fig2: Short Circuit Current Test Circuit

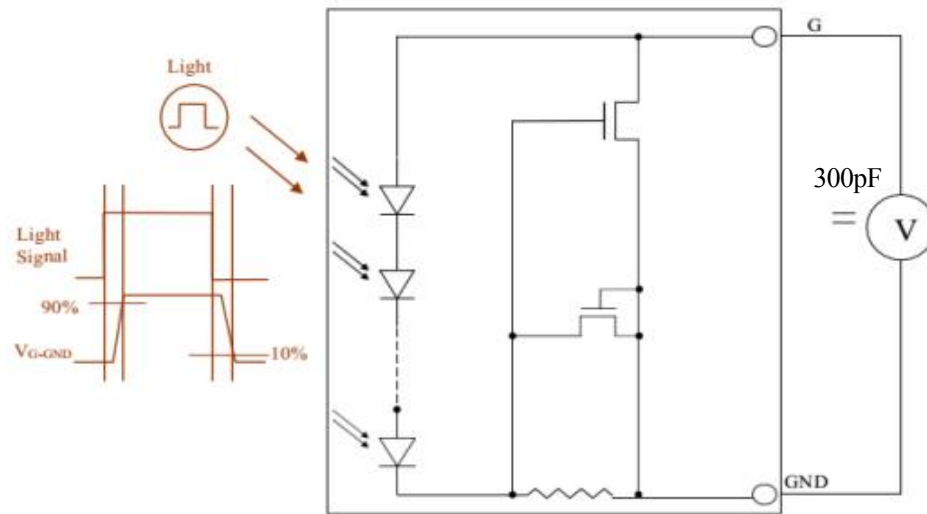


Fig3: T_{on}/T_{off} TEST Circuit

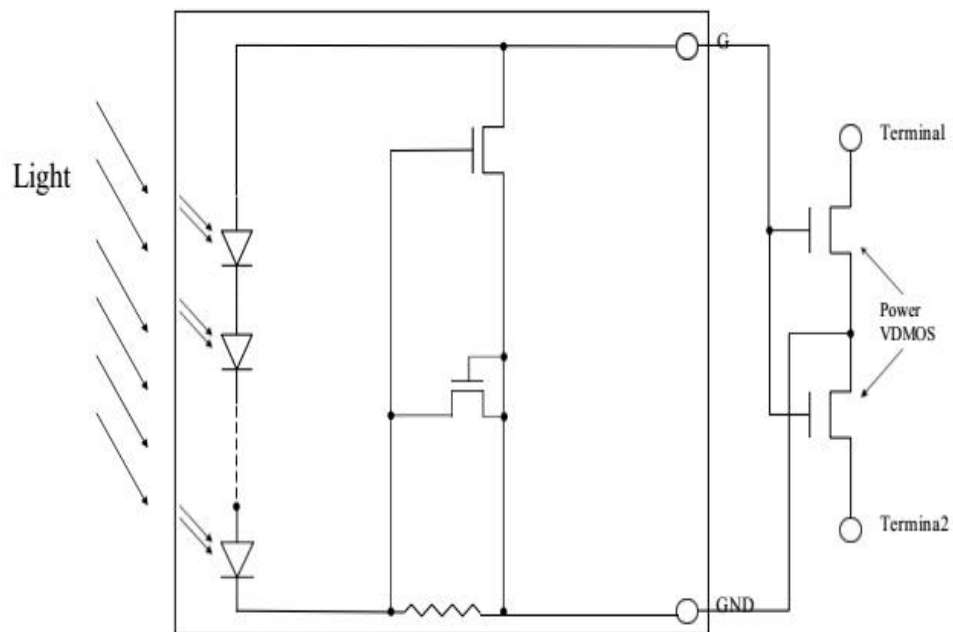


Fig4: Application Circuit

PAD Layout

光伏样品 PAD 示意图，芯片尺寸：X=1420um Y=1440um

