

Overview

Feature

- Skin Detector to perform precise in-ear detection
- Integrated 1050nm LED, 1450nm LED, SWIR PD & ASIC
- Crosstalk and ambient light cancellation
- Wide configuration range
- VDD wide operation range 1.7~2.0v
- 1.8V Power Supply with 1.8V~3.6V I²C bus
- ELP3601 fully comply with current RoHS directives

Application

- Wearable product for power control
- TWS Earbuds

Description

In light of the increasingly popular wide spectrum (NIR/SWIR) optical sensing applications in skin detection in TWS ear buds, optical components including LED, and SWIR sensors have become the crucial factors

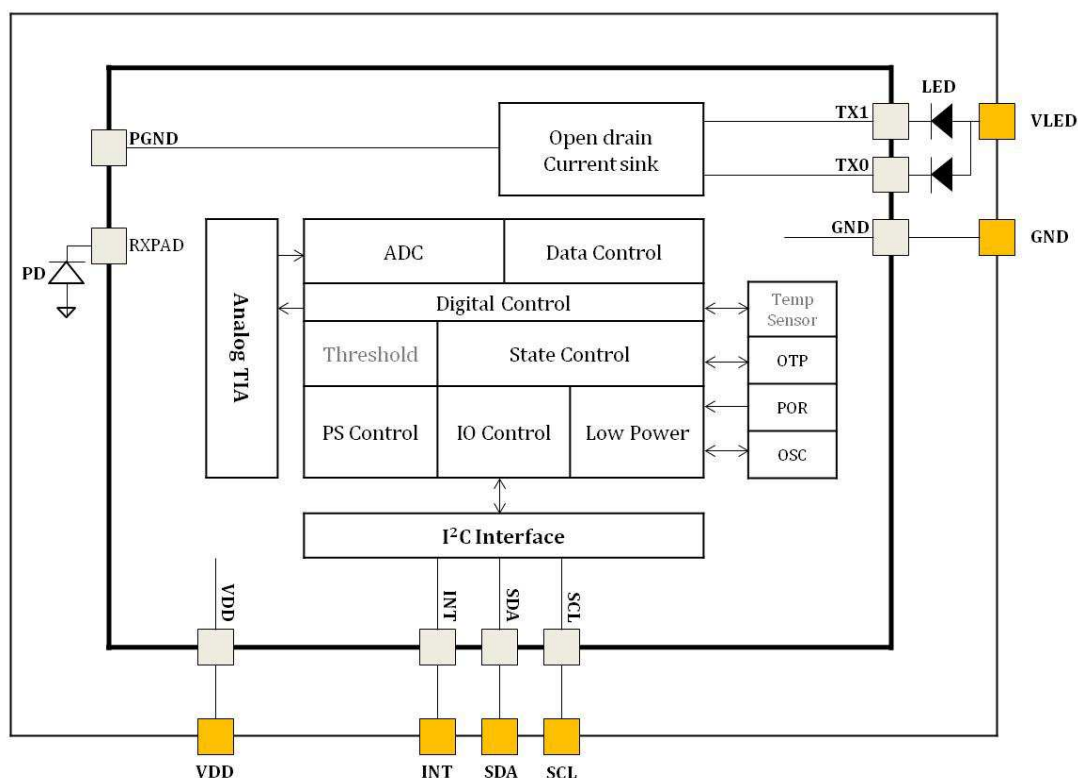
to meet such rising user demands. The widely discussed skin detection function in TWS earbuds requires SWIR sensors to perform precise in-ear detection and to deliver seamless listening experiences, while at the same time sustaining long battery life. Such product requires SWIR wavelength, lower power-consumption, lower cost and smaller size with higher sensitivity.

The ELP3601 features Skin Sensor with 2mm x 1mm x 0.65mm package. This device incorporates 1050nm & 1450nm LED and SWIR PD. The device provides skin detection by ratio of reflected 1050nm and 1450nm IR light from LED.

The ELP3601 incorporates SWIR PD, timing control, ADC and LED into one chip. The device provides excellent proximity detection. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor.

The ELP3601 has provided temperature calibration features and also has lower power design, including standby mode and wait mode support.

Block Diagram



Pin Description

Description

Name	Pin No.	IO	Description
INT	1	IO	Interrupt pin (open drain)
VDD	2	P	Power supply:1.7v~2.0v
GND	3	G	Ground
VDD3	4	P	Supply Voltage for IR emitter (2.4v~3.6v)
SCL	5	I	IIC clock
SDA	6	IO	IIC data (open drain)

Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	Supply Voltage to GND	-0.3	2.0	V	
VDD3	IR emitter Voltage to GND	-0.3	3.6	V	
V _{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	
I _{IO}	Digital Output TerminalCurrent	-1	20	mA	
Electrostatic Discharge					
I _{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78E
ESD _{HBM}	HBM ElectrostaticDischarge	± 2000		V	JEDEC/ESDA JS-001-2017
ESD _{CDM}	CDM ElectrostaticDischarge	± 500		V	JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
T _{STRG}	Storage TemperatureRange	-40	85	°C	
T _{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) isspecified according to IPC/JEDEC J-STD-020 “Moisture/ReflowSensitivity Classification for Non-hermetic Solid State SurfaceMount Devices.”
RH _{NC}	Relative Humidity (non-condensing)		85	%	
P _{DISS}	Power Dissipation		50	mW	Average power dissipation over a1 second period

■ Recommended Operation condition

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage to Sensor	1.7	1.8	1.98	V
VDD3	Supply Voltage to IR emitter	2.4	3.3	3.6	V
f _{I2C}	Clock frequency of I ² C	-	-	400	kHz
T _A	Operating Ambient Temperature	-30		85	°C

■ Electrical and Proximity sensor characteristics

■ Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD}	Supply current	Active State (PON=1) ⁽¹⁾		568		μA
		Active State (PON=1) ⁽²⁾		22		
		Idle State (PON=1)		26		
		Sleep State (PON = 0) ⁽³⁾		0.15		
V _{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I _{LEAK}	Leakage current, SDA, SCL, INT		-5		5	μA
V _{IH}	SCL, SDA input high voltage ⁽⁴⁾		1.26			V
V _{IL}	SCL, SDA input low voltage				0.54	V
T _{Active}	Time from power-on to ready to receive I ² C commands			1.5		ms

Note(s):

1. Active state occurs when PON = 1, P0EN = 1, P1EN = 1 and the device is actively integrating. For the PS operation, 16 pulse with 16pulse width at 1.39ms measurement time.
2. Active state occurs when PON = 1, P0EN = 1, P1EN = 1 and the device is actively integrating. For the PS operation, 16 pulse with 16pulse width at 200ms measurement time, this is by the wait time(WTIME).
3. Sleep state occurs when PON = 0 and I²C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
4. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.6V

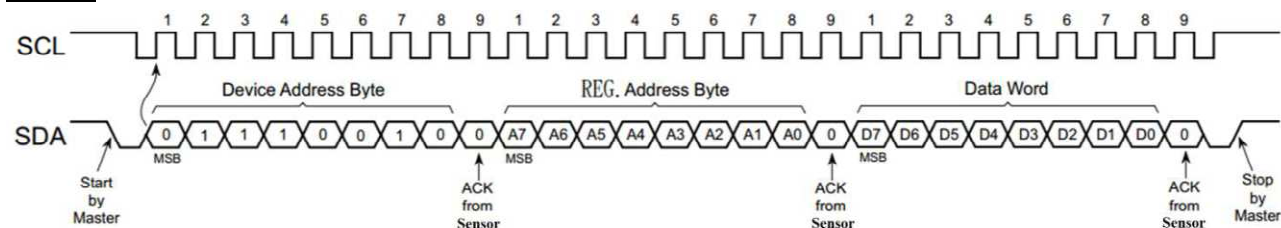
■ Proximity sensor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Peak wavelength for LED0			1050		nm
Peak wavelength for LED1			1450		nm
PS _{FS}				4096	Counts
LED pulse current		8		30	mA
LED pulse width		5	16	64	us
Numbers of LED pulse		1	16	64	pulse

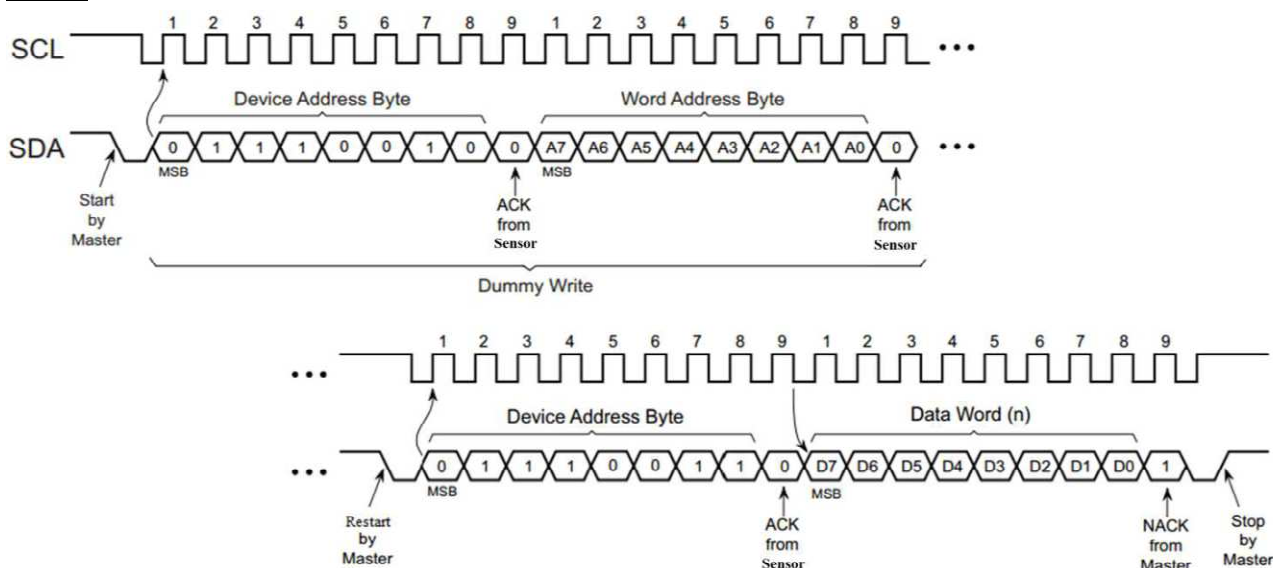
I2C Timing Diagram

IIC Communication

Write:



Read:



Register Description

■ Register table

Address	Register Name	R/W	Register Function	ResetValue
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x82	PRATE	R/W	Proximity time	0x00
0x84	PILT0L	R/W	LED0 interrupt low threshold low byte	0x00
0x85	PILT0H	R/W	LED0 interrupt low threshold high byte	0x00
0x86	PIHT0L	R/W	LED0 interrupt high threshold low byte	0x00
0x87	PIHT0H	R/W	LED0 interrupt high threshold high byte	0x00
0x88	PILT1L	R/W	LED1 interrupt low threshold low byte	0x00
0x89	PILT1H	R/W	LED1 interrupt low threshold high byte	0x00
0x8A	PIHT1L	R/W	LED1 interrupt high threshold low byte	0x00
0x8B	PIHT1H	R/W	LED1 interrupt high threshold high byte	0x00
0x8C	PERS	R/W	Proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x50
0x8E	PCFG0	R/W	Proximity configuration zero	0x8F
0x8F	PCFG1	R/W	Proximity configuration one	0x60
0x90	CFG1	R/W	Configuration one	0x40
0x91	PCFG2	R/W	Proximity configuration two	0x0A
0x92	ID	R	Device ID	0x44
0x93	PPULSE_LENH	R/W	Pulse length high byte value	0x00
0x94	PPULSE_LENL	R/W	Pulse length low byte value	0x20
0x9A	STATUS0	R, SC	Device interrupt status byte0	0x00
0x9B	STATUS1	R, SC	Device interrupt status byte1	0x00
0x9C	PDATA0L	R	LED0 emitted period ADC low data	0x00
0x9D	PDATA0H	R	LED0 emitted period ADC high data	0x00
0x9F	PDATA1L	R	LED1 emitted period ADC low data	0x00
0xA0	PDATA1H	R	LED1 emitted period ADC high data	0x00
0xA6	REVID2	R	Revision ID two	0x01
0xA8	SOFT_RST	R/W	Soft reset	0x00
0xA9	PWTIME	R/W	Proximity wait time	0x00

0xAA	CFG8	R/W	Configuration eight	0x00
0xAB	CFG3	R/W	Configuration three	0x04
0xB3	PFILTER	R/W	Proximity filter	0x00
0xC0	POFFSET0L	R/W	LED0 emitted period offset low data	0x00
0xC1	POFFSET0H	R/W	LED0 emitted period offset high data	0x00
0xC2	POFFSET1L	R/W	LED1 emitted period offset low data	0x00
0xC3	POFFSET1H	R/W	LED1 emitted period offset high data	0x00
0xD7	CALIB	R/W	Proximity offset calibration	0x00
0xD9	CALIBCFG0	R/W	Proximity offset calibration control 0	0x50
0xDA	CALIBCFG1	R/W	Proximity offset calibration control 1	0x40
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00
0xF4	PS_SWCFG2	R/W	Proximity configuration two	0x73
0xF6	PS0DA	R/W	LED0 emitted period offset calibration	0x60
0xF7	PS1DA	R/W	LED1 emitted period offset calibration	0x60
0xF8	HDRCFG	R/W	HDR configuration	0x00
0x79	TRCODE	R/W	Trace code	0x00

Detail of Register Description

■ Enable register (Address 0x80)

Addr: 0x80		Enable		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	RW	Reserved
4	PWEN	0	RW	This bit activates the proximity wait feature which is set by the PWTIME register. Active high.
3	Reserved	0	RW	Reserved
2	P1EN	0	RW	This bit activates the LED1 proximity detection. Active high.
1	P0EN	0	RW	This bit activates the LED0 proximity detection. Active high.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

■ PRATE register (Address 0x82)

Addr:0x82		PRATE		
Bit	Bit Name	Default	Access	Bit Description
7:0	PRATE	0x00	RW	PS Integration Time Value The PRATE value specifies the PS integration time in 1.39ms intervals. 0x00 indicates 1.39ms. The maximum PS count value depends on the integration time.

■ PILT0L Register (Address 0x84)

Addr: 0x84		PILT0L		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILT0L	0x00	RW	PS0 Low Threshold Value This register contains the low byte of the 12-bit proximity 0 LOW threshold.

■ PILT0H Register (Address 0x85)

Addr: 0x85		PILT0H		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILT0H	0x00	RW	PS0 Low Threshold Value This register contains the upper 4-bits of the 12-bit proximity 0 LOW threshold.

■ PIHT0L Register (Address 0x86)

Addr: 0x86		PIHT0L		
Bit	Bit Name	Default	Access	Bit Description
7:0	PIHT0L	0x00	RW	PS0 High Threshold Value This register contains the low byte of the 12-bit proximity 0 HIGH threshold.

■ PIHT0H Register (Address 0x87)

Addr: 0x87		PIHT0H		
Bit	Bit Name	Default	Access	Bit Description
7:0	PIHT0H	0x00	RW	PS High Threshold Value This register contains the upper 4-bits of the 12-bit proximity 0 HIGH threshold.

■ PILT1L Register (Address 0x88)

Addr: 0x88		PILT1L		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILT1L	0x00	RW	PS1 Low Threshold Value This register contains the low byte of the 12-bit proximity 1 LOW threshold.

■ PILT1H Register (Address 0x89)

Addr: 0x89		PILT0H		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILT1H	0x00	RW	PS1 Low Threshold Value This register contains the upper 4-bits of the 12-bit proximity 1 LOW threshold.

■ PIHT1L Register (Address 0x8A)

Addr: 0x8A		PIHT0L		
Bit	Bit Name	Default	Access	Bit Description
7:0	PIHT1L	0x00	RW	PS1 High Threshold Value This register contains the low byte of the 12-bit proximity 1 HIGH threshold.

■ PIHT1H Register (Address 0x8B)

Addr: 0x8B		PIHT0H		
Bit	Bit Name	Default	Access	Bit Description

7:0	PIHT1H	0x00	RW	PS1 High Threshold Value This register contains the upper 4-bits of the 12-bit proximity 1 HIGH threshold.
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■ PERS Register (Address 0x8C)

Addr: 0x8C		PERS		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	--	Reserved.
3:0	PERS	0000	RW	This register sets the PS persistence filter.
				0 (0000) Every PS cycle
				1 (0001) Any value outside PS thresholds
				2 (0010) 2 consecutive PS values out of range
				3 (0011) 3 consecutive PS values out of range
				4 (0100) 4 consecutive PS values out of range
				5 (0101) 5 consecutive PS values out of range
				6 (0110) 6 consecutive PS values out of range
				7 (0111) 7 consecutive PS values out of range
				
				13 (1101) 13 consecutive PS values out of range
				14 (1110) 14 consecutive PS values out of range
				15 (1111) 15 consecutive PS values out of range

■ CFG0 Register (Address 0x8D)

Addr: 0x8D		CFG0		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0101	RW	Reserved. Must be set to default value.
3	PWLONG	0	RW	PS Wait Long Flag The PWTIME is increased by a factor of 16 when PWLONG is asserted. PWLONG = 1, PWTIME = PWTIME x 16 PWLONG = 0, PWTIME = PWTIME x 1
2:0	Reserved	000	RW	Reserved. Must be set to default value.

■ PCFG0 Register (Address 0x8E)

Addr: 0x8E		PFCG0		
Bit	Bit Name	Default	Access	Bit Description
7:6	POGAIN1	10	RW	PS0 Gain1 Value PGAIN1 = 0, 1x gain. PGAIN1 = 1, 2x gain. PGAIN1 = 2, 4x gain. PGAIN1 = 3, 8x gain.
5:0	PPULSE	001111	RW	PS Pulse Number Value The PPULSE sets the maximum number of pulses in a single proximity cycle. Max. pulse number=64

■ PCFG1 Register (Address 0x8F)

Addr: 0x8F		PFCG1			
Bit	Bit Name	Default	Access	Bit Description	
7:4	Reserved	0000	--	Reserved.	
3:0	PLDRIVE0	0000	RW	PS0 Pulse Drive Current The drive strength of the IR LED0 current is set by the field	
				PLDRIVE0	LED Current
				0000	8mA
				0001	11mA
				0010	15mA
				0011	18mA
				0100	21mA
				0101	24mA
				0110	27mA
				0111	30mA

■ CFG1 Register (Address 0x90)

Addr: 0x90		CFG1		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	--	Reserved.
6:5	POGAIN2	10	RW	PS0 Gain2 Value PGAIN2 = 0, 1.25x gain. PGAIN2 = 1, 2.5x gain. PGAIN2 = 2, 5x gain. PGAIN2 = 3, 10x gain.
4	Reserved	0	--	Reserved.

3:0	PLDRIVE1	0000	RW	PS1 Pulse Drive Current	
				The drive strength of the IR LED1 current is set by the field	
				PLDRIVE1	LED Current
				0000	8mA
				0001	11mA
				0010	15mA
				0011	18mA
				0100	21mA
				0101	24mA
				0110	27mA
				0111	30mA

■ PCFG2 Register (Address 0x91)

Addr: 0x91		PCFG2		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	--	Reserved.
3:2	P1GAIN1	10	RW	PS1 Gain1 Value P1GAIN1 = 0, 1x gain. P1GAIN1 = 1, 2x gain. P1GAIN1 = 2, 4x gain. P1GAIN1 = 3, 8xgain
1:0	P1GAIN2	10	RW	PS1 Gain2 Value PGAIN2 = 0, 1.25x gain. PGAIN2 = 1, 2.5x gain. PGAIN2 = 2, 5x gain. PGAIN2 = 3, 10x gain.

■ ID Register (Address 0x92)

Addr: 0x92		ID		
Bit	Bit Name	Default	Access	Bit Description
7:2	ID	010001	RO	Device type identification.
1:0	Reserved	00	RO	Reserved.

■ PPULSE_LENH Register (Address 0x93)

Addr: 0x93		PPULSE_LENH		
Bit	Bit Name	Default	Access	Bit Description

7:2	Reserved	000000	--	Reserved.
1:0	PPULSE_LENH	00	RW	PS Pulse Length High Byte Value These bits are the 2 most significant bits of the 10-bit pulse length control setting. The lower 8 bits are in the PPULSE_LENH register. The minimum pulse length is 5μs.

■ PPULSE_LENH Register (Address 0x94)

Addr: 0x94		PPULSE_LENH		
Bit	Bit Name	Default	Access	Bit Description
7:0	PPULSE_LENH	0x20	RW	PS Pulse Length Low Byte Value These bits are the 8 least significant bits of the 10-bit pulse length control setting. The higher 2 bits are in the PPULSE_LENH register. The minimum pulse length is 5μs.

■ STATUS0 Register (Address 0x9A)

Addr: 0x9A		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	000	--	Reserved.
5	TINT	0	R, SC	Temperature Interrupt Flag If the temperature inside ELP3601 goes out of range, this flag will be set to indicate the temperature has changed.
4	PINT	0	R, SC	PS Interrupt Flag If P0EN is set, proximity interrupt flag indicates that proximity 0 results have exceeded thresholds and persistence settings. Alternatively, if P1EN is set, it indicates that proximity 1 results have exceeded threshold and persistence.
3	PSAT	0	R, SC	PS Saturation Flag Proximity saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle. (Note : PS_IR data = 12'h000 or PS_EM data = 12'h000 including hardware average)
2	CINT	0	R, SC	Calibration Interrupt Flag Calibration interrupt flag indicates that calibration has completed.

1	ZINT	0	R,SC	PS Zero Detection Flag If P0EN is set, zero detection interrupt flag indicates that a zero value in proximity 0. Alternatively, If P1EN is set, zero detection interrupt flag indicates that a zero value in proximity 1. If AUTO_OFFSET_ADJ is set, it caused the proximity offset to be decremented.
0	Reserved	0	--	Reserved.

■ STATUS1 Register (Address 0x9B)

Addr: 0x9B		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7	P1INT	0	R, SC	PS1 Interrupt Flag Proximity interrupt flag indicates that LED1 proximity results have exceeded thresholds and persistence settings.
6	Z1INT	0	R, SC	PS1 Zero Detection Flag Zero detection interrupt flag indicates that a zero value in PDATA has caused the LED1 proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
5	P1SAT_REF	0	R, SC	PS Reflective LED1 Proximity Saturation Flag The Reflective LED1 Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED1 active portion of proximity integration.
4	P1SAT_AMB	0	R,SC	PS Ambient LED1 Proximity Saturation Flag The Ambient LED1 Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED1 inactive portion of proximity integration.
3	P0INT	0	R,SC	PS0 Interrupt Flag Proximity interrupt flag indicates that LED0 proximity results have exceeded thresholds and persistence settings.
2	Z0INT	0	R,SC	PS0 Zero Detection Flag Zero detection interrupt flag indicates that a zero value in PDATA has caused the LED0 proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
1	P0SAT_REF	0	R,SC	PS Reflective LED0 Proximity Saturation Flag The Reflective LED0 Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED0 active portion of

				proximity integration.
0	POSAT_AMB	0	R,SC	PS Ambient LED0 Proximity Saturation Flag The Ambient LED0 Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR LED0 inactive portion of proximity integration.

■ PDATA0L Register (Address 0x9C)

Addr: 0x9C		PDATAL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PDATA0L	0x00	RO	PS0 Low Byte Data (PS_A_Data) This register contains the low byte of the 12-bit proximity ADC data.

■ PDATA0M Register (Address 0x9D)

Addr: 0x9D		PDATAM		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	RO	Reserved.
3:0	PDATA0H	0000	RO	PS0 High Data (PS_A_Data) This register contains the 4 most significant bits of the 12-bit proximity ADC data.

■ PDATA1L Register (Address 0x9F)

Addr: 0x9F		PDATAL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PDATA1L	0x00	RO	PS1 Low Byte Data (PS_A_Data) This register contains the low byte of the 12-bit proximity ADC data.

■ PDATA1H Register (Address 0xA0)

Addr: 0xA0		PDATAM		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	RO	Reserved.
3:0	PDATA1H	0000	RO	PS1 High Data (PS_A_Data) This register contains the 4 most significant bits of the 12-bit proximity ADC data.

■ REVID2 Register (Address 0xA6)

Addr: 0xA6		REVID2		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	--	Reserved.
3:0	VER_ID	0001	RO	Device Version Number

■ SOFTRST Register (Address 0xA8)

Addr: 0xA8		IRM		
Bit	Bit Name	Default	Access	Bit Description
7:1	Reserved	0000000	--	Reserved
0	SOFTRST	0	R/W	Software Reset Enable Flag Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state. SOFTRST = 1, All registers will be reset to the default state. SOFTRST = 0, Normal operation.

■ PWTIME Register (Address 0xA9)

Addr: 0xA9		PWTIME				
Bit	Bit Name	Default	Access	Bit Description		
7:0	PWTIME	0x00	RW	PS Wait Time Value The PWTIME value specifies the PS wait time in 1.39ms intervals. 0x00 indicates 1.39ms.		
				PWTIME	Wait Cycles	Wait Time
				0x00	1	1.39ms
				0x01	2	2.78ms
				0x11	18	25ms
				0x23	36	50ms
						
				0x3F	64	89ms
						
				0xFF	256	356ms

■ CFG8 Register (Address 0xAA)

Addr: 0xAA		CFG8		
Bit	Bit Name	Default	Access	Bit Description
7:1	Reserved	0000000	--	Reserved.

0	PDEN	0	RW	Proximity PD Enable Flag
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■ CFG3 Register (Address 0xAB)

Addr: 0xAB		CFG3					
Bit	Bit Name	Default	Access	Bit Description			
7	INTRD_CLEAR	0	RW	Status Reset Flag If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over I2C. INTRD_CLR = 1, All flag bits of the STATUS register are reset. INTRD_CLR = 0, IDLE.			
6:5	Reserved	00	--	Reserved.			
4	SAI	0	RW	Sleep After Interrupt Enable Flag The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pinassertion.			
				PON	SAI	INT	Oscillator
				0	X	X	OFF
				1	0	X	ON
				1	1	1	ON
				1	1	0	OFF
3:0	Reserved	0100	RW	Reserved. Must be set to default value.			

■ PFILTER Register (Address 0xB3)

Addr: 0xB3		PFILTER			
Bit	Bit Name	Default	Access	Bit Description	
7:2	Reserved	000000	--	Reserved.	
1:0	PMAVG	00	RW	Proximity Moving average selection Flag	
				PMAVG	MAV Select
				00	Disabled
				01	2 Values
				10	4 Values

■ POFFSET0L Register (Address 0xC0)

Addr: 0xC0		POFFSET0L		
Bit	Bit Name	Default	Access	Bit Description

7:0	POFFSET0L	0x00	RW	Proximity0 Crosstalk Offset Low Byte This register contains the low byte of the signed proximity0 offset adjust value.
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■ POFFSET0H Register (Address 0xC1)

Addr: 0xC1		POFFSET0H		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved.
4:0	POFFSET0H	00000	RW	Proximity0 Crosstalk Offset High Byte This register contains the 5 most significant bits of the signed proximity0 offset adjust value.

■ POFFSET1L Register (Address 0xC2)

Addr: 0xC2		POFFSET1L		
Bit	Bit Name	Default	Access	Bit Description
7:0	POFFSET1L	0x00	RW	Proximity1 Crosstalk Offset Low Byte This register contains the low byte of the signed proximity1 offset adjust value.

■ POFFSET1H Register (Address 0xC3)

Addr: 0xC3		POFFSET1H		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	--	--	Reserved.
4:0	POFFSET1H	0	RW	Proximity1 Crosstalk Offset High Byte This register contains the 5 most significant bits of the signed proximity1 offset adjust value.

■ CALIB Register (Address 0xD7)

Addr: 0xD7		CALIB		
Bit	Bit Name	Default	Access	Bit Description
7	CALAVG	0	RW	Calibration Average Enable Flag Enables proximity hardware averaging as selected with PROX_AVG during calibration. CALAVG = 0, No hardware averaging CALAVG = 1, Hardware averaging enabled
6:5	Reserved	00	--	Reserved.
4	CALPRAT	0	RW	Calibration PRATE Enable Flag

	E			Enables PRATE during calibration. Useful when averaging is enabled. CALPRATE = 0, PRATE ignored CALPRATE = 1, PRATE applied between averaging samples
3:1	Reserved	000	--	Reserved.
0	START_OFFSET_CAL	0	RW	Calibration Start Flag Calibration sequence start. START_OFFSET_CAL = 1, Calibration start. START_OFFSET_CAL = 0, IDLE.

■ CALIBCFG0 Register (Address 0xD9)

Addr: 0xD9		CALIBCFG0		
Bit	Bit Name	Default	Access	Bit Description
7:5	BINSRCH_TARGET0	010	RW	Proximity Offset Calibration Target
				Value PDATA Target
				(000)0 3
				(001)1 7
				(010)2 15
				(011)3 31
				(100)4 63
				(101)5 127
				(110)6 255
				(111)7 511
4	Reserved	1	--	Reserved. Must be set to default value.
3	AT_OFS_ADJ	0	RW	Auto Offset Adjustment If set, this bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero.
2:0	PROX_AVG	000	RW	PS Hardware Average Number PROX_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.
				Value Averaging Cycle
				(000)0 Disable
				(001)1 2
				(010)2 4

				(011)3	8
				(100)4	16
				(101)5	32
				(110)6	64
				(111)7	128

■ CALIBCFG1 Register (Address 0xDA)

Addr: 0xDA		CALIBCFG1		
Bit	Bit Name	Default	Access	Bit Description
7:5	BINSRCH_TARGET1	010	RW	Proximity Offset Calibration Target
				Value PDATA Target
				(000)0 3
				(001)1 7
				(010)2 15
				(011)3 31
				(100)4 63
				(101)5 127
				(110)6 255
				(111)7 511
4:0	Reserved	00000	--	Reserved. Must be set to default value.

■ CALIBSTAT Register (Address 0xDC)

Addr: 0xDC		CALIBSTAT		
Bit	Bit Name	Default	Access	Bit Description
7:4	Reserved	0000	--	Reserved.
3	OFFSET1_ADJUSTED	0	RW	PS1 Offset Adjusted Enable Flag Bit is set when the proximity1 offset has been automatically decremented if AUTO_OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_OFFSET_ADJ to 0.
2	OFFSET0_ADJUSTED	0	RW	PS0 Offset Adjusted Enable Flag Bit is set when the proximity0 offset has been automatically decremented if AUTO_OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting

				AUTO_OFFSET_ADJ to 0.
1	Reserved	0	--	Reserved.
0	CALIB_FI NISHED	0	RW	Calibration finish flag This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

■ INTENAB Register (Address 0xDD)

Addr: 0xDD		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	00	--	Reserved.
5	TIEN	0	RW	Temperature Interrupt Enable Flag
4	PIEN	0	RW	PS Interrupt Enable Flag
3	PSIEN	0	RW	PS Saturation interrupt Enable Flag
2	CIEN	0	RW	Calibration Interrupt Enable Flag
1	ZIEN	0	RW	Zero detect Interrupt Enable Flag
0	Reserved	0	--	Reserved.

■ PS_SWCFG2 Register (Address 0xF4)

Addr: 0xF4		PS_SWCFG2		
Bit	Bit Name	Default	Access	Bit Description
7	EN_COMP _PS	0	RW	Enable/Disable crosstalk compensation using P0RS, P1RS, P0DA and P1DA.
6:0	Reserved	1110011	--	Reserved. Must be set to default value.

■ PS0DA Register (Address 0xF6)

Addr: 0xF6		PS0DA		
Bit	Bit Name	Default	Access	Bit Description
7:6	P0RS	01	RW	PS0 Offset Calibration DA Stage Flag
5:0	P0DA	100000	RW	PS1 Offset Calibration DA Selection Flag

■ PS1DA Register (Address 0xF7)

Addr: 0xF7		PS1DA		
Bit	Bit Name	Default	Access	Bit Description
7:6	P1RS	01	RW	PS1 Offset Calibration DA Stage Flag

5:0	P1DA	100000	RW	PS1 Offset Calibration DA Selection Flag
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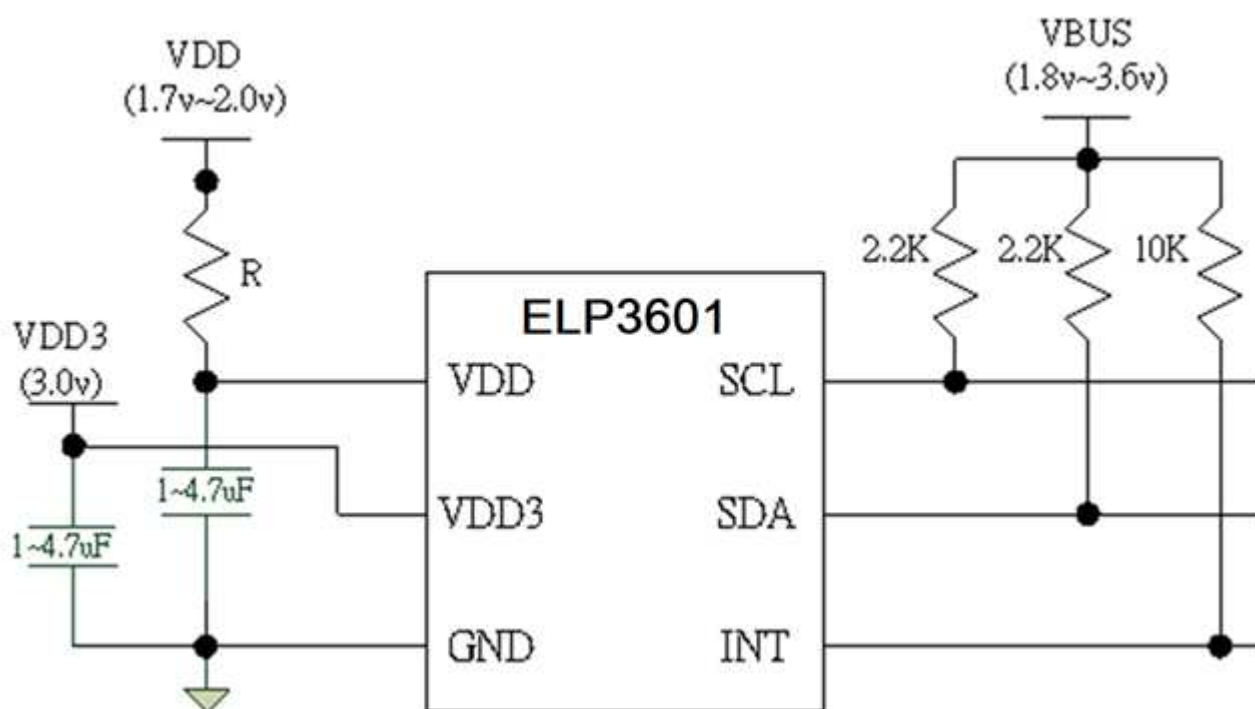
■ HDRCFG Register (Address 0xF8)

Addr: 0xF8		HDRCFG		
Bit	Bit Name	Default	Access	Bit Description
7:6	P1DA_BAS E	00	RW	PS1 Offset Calibration DA Basement Flag
5:4	P0DA_BAS E	00	RW	PS0 Offset Calibration DA Basement Flag
3:0	Reserved	0011	--	Reserved. Must be set to default value.

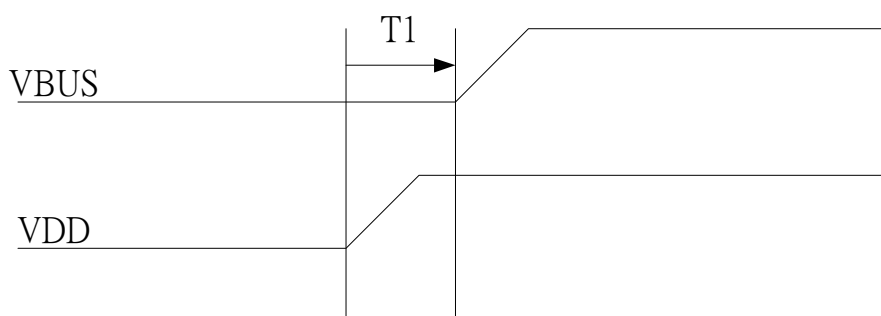
■ TRCODE Register (Address 0x79)

Addr: 0x79		TRCODE		
Bit	Bit Name	Default	Access	Bit Description
7:5	Reserved	000	--	Reserved. Must be set to default value.
4:0	TRCODE	00000	R	Trace code

Application Circuit



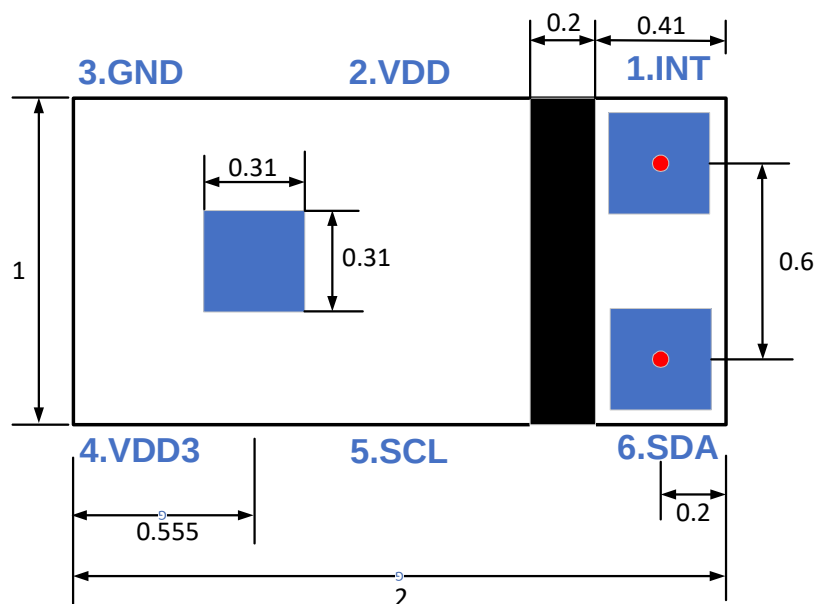
Power on Sequence



Note: The T1 time is recommended more than 30ms (VDD first is recommended)

Package Information

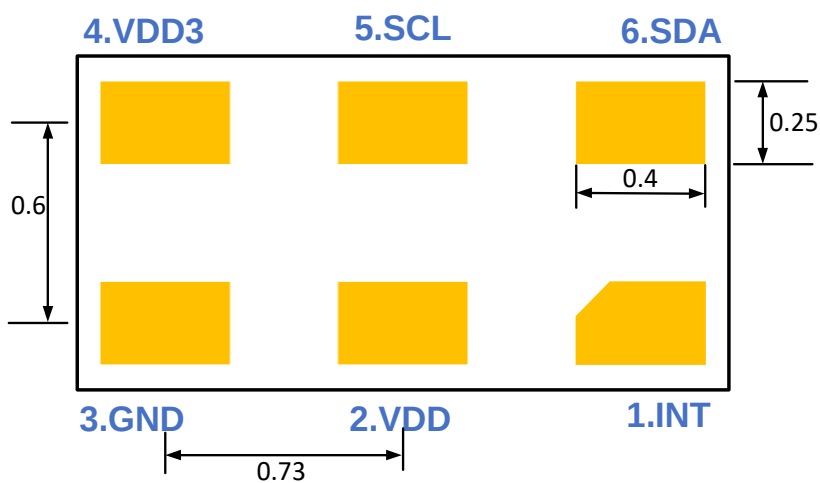
TOP View



Side View



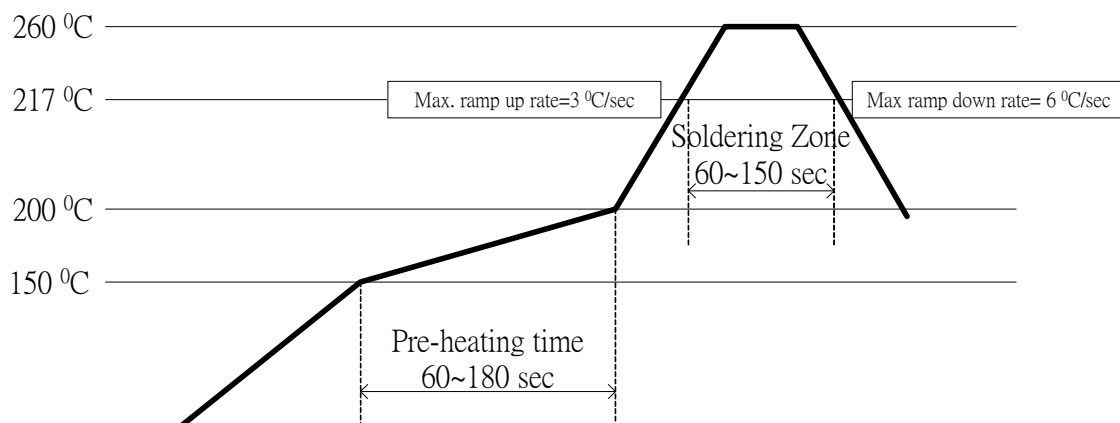
Bottom View



Note: all dimensions are in mm

Soldering Information

■ Soldering condition



Note ¹: Reflow soldering should not be done more than three times

Note ²: When soldering, do not stress on IC during heating

Note ³: After soldering, do not warp the board

Recommended of storage method and ESD precaution

Dry box storage is recommended as soon as the aluminum bag has been opened. It could prevent moisture absorption.
The following conditions should be followed if dry boxes are not available

- Storage temperature 10C to 30C
- Storage humidity <= 60% RH max

After more than 72 hours Under the conditions moisture content will be too high for reflow soldering. In case of moisture absorption, the devices will recover to former conditions by drying under the following condition

- 192 hours at 40C and 5% RH or
- 96 hours at 60C and < 5% RH for device containers, or
- 24 hours at 125C is not suitable for reel

ESD precaution

- When the Chips are removed from Anti-static bag, please follow the handing procedure to prevent ESD damage